AMENDMENTS TO THE CLAIMS

1-9. (Canceled)

10. (Currently Amended) A SIMD processor for executing SIMD instructions, the SIMD processor comprising:

a first register operable to store data;

a second register operable to store data;

a flag storage unit operable to store a first flag;

a decoding unit operable to decode an instruction; and

an execution unit operable to execute the instruction based on a result of the decoding performed by the decoding unit,

wherein the execution unit, when the decoding unit decodes an instruction for performing a SIMD operation, the instruction including operands specifying [[a]] the first register and [[a]] the second register, refers to the first flag stored in the flag storage unit, and performs the SIMD operation (i) only on the operand held in the first register when the first flag stored in the flag storage unit indicates a first status, and (ii) on the operands held in the first register and the second register when the first flag indicates a second status.

11. (Currently Amended) The SIMD processor according to Claim 10,

wherein the SIMD operation is addition, and

wherein the execution unit adds (i) a value held in the first register and said value held in the first register when the first flag indicates the first status, and (ii) the value held in the first register and a value held in the second register when the first flag indicates the second status.

12. (Original) The SIMD processor according to Claim 11,

wherein the execution unit, when two pieces of data a1 and a2 are stored in the first register and two pieces of data b1 and b2 are stored in the second register, calculates (i) (a1+a1) and (a2+a2) when the first flag indicates the first status, and (ii) (a1+b1) and (a2+b2) when the first flag indicates the second status.

13. (Currently Amended) A SIMD processor for executing SIMD instructions, the SIMD processor comprising:

a first register operable to store data;

a second register operable to store data;

a flag storage unit operable to store a flag;

a decoding unit operable to decode an instruction; and

an execution unit operable to execute the instruction based on a result of the decoding performed by the decoding unit,

wherein the execution unit, when the decoding unit decodes an instruction for performing a SIMD operation, the instruction including operands specifying [[a]] the first register and [[a]] the second register, refers to the flag stored in the flag storage unit, and performs the SIMD

operation (i) only on the operand held in the first register and rounds an operation result when the flag stored in the flag storage unit indicates a first status, and (ii) on the operands held in the first register and the second register and rounds an operation result when the flag indicates a second status.

14. (Currently Amended) The SIMD processor according to Claim 13,

wherein the SIMD operation is addition, and

wherein the execution unit adds (i) a value held in the first register and said value held in the first register, and adds 1 to an addition result when the flag indicates the first status, and (ii) the value held in the first register and a value held in the second register, and adds 1 to an addition result when the flag indicates the second status.

15. (Original) The SIMD processor according to Claim 14,

wherein the execution unit, when two pieces of data a1 and a2 are stored in the first register and two pieces of data b1 and b2 are stored in the second register, calculates (i) (a1+a1+1) and (a2+a2+1) when the flag indicates the first status, and (ii) (a1+b1+1) and (a2+b2+1) when the flag indicates the second status.

16. (Currently Amended) The SIMD processor according to Claim 10,

wherein the flag storage unit further stores a second flag, and

wherein the execution unit determines whether to round the operation result or not depending on a value of the second flag.

17. (Original) The SIMD processor according to Claim 11,

wherein the execution unit further divides the operation result by 2.

18-55. (Canceled)

56. (New) The SIMD processor according to claim 10, wherein the first status of the first flag is either "0" or "1".

57. (New) The SIMD processor according to claim 13, wherein the first status of the flag is either "0" or "1".